CLAIMS

1. A cache memory having a conditional access mechanism operated by a locking condition, for conditionally locking said cache memory.

2. A cache memory according to claim 1, wherein said conditional access mechanism comprises:

a condition checker, for determining fulfillment of said locking condition;

a hit determiner, for giving hit and miss indications for data stored in said cache memory; and

a cache accessor, for conditionally implementing a cache memory access in accordance with the fulfillment of said locking condition.

3. A cache memory according to claim 2, wherein said conditional implementing comprises accessing said cache memory with cached data locked if said locking condition is fulfilled.

4. A cache memory according to claim 1, wherein said conditional access mechanism is operable to prevent replacement of data stored in a section of a conditionally locked cache memory.

5. A cache memory according to claim 1, wherein said conditional access mechanism is operable to update data stored in a section of a conditionally locked cache memory.

6. A cache memory according to claim 1, wherein said conditional access mechanism is operable to prevent reallocation of a section of a conditionally locked cache memory.

7. A cache memory according to claim 1, wherein said conditional access mechanism is operable to access a section of a conditionally unlocked cache memory, in accordance with a corresponding lock bit.

8. A cache memory according to claim 1, further comprising a condition definer, for holding a definition of said locking condition.

9. A cache memory according to claim 8, wherein said definition is updateable during operation.

10. A cache memory according to claim 8, wherein said definition comprises a condition type and parameters associated with said type.

11. A cache memory according to claim 1, wherein said locking condition is fulfilled if a currently accessed main memory location comprises a main memory location specified by said locking condition.

12. A cache memory according to claim 1, wherein each main memory access instruction has a type, and wherein said locking condition is fulfilled if a type of said memory access command comprises a command type specified by said locking condition.

13. A cache memory according to claim 1, wherein said cache memory comprises a conditional locking indicator, and wherein said locking condition is fulfilled if said conditional locking indicator is set.

14. A cache memory according to claim 1, wherein said memory access command comprises a conditional locking parameter, for turning on conditional locking during the execution of said command.

15. A cache memory according to claim 1, wherein said accessor is operable to turn conditional accessing on and off in accordance with a predetermined memory access command.

16. A cache memory according to claim 1, wherein said cache memory is for caching data of an associated main memory.

17. A cache memory according to claim 16, wherein said cache memory is further associated with a processor operable to access said associated main memory via said cache memory.

18. A cache memory according to claim 17, wherein said locking condition is fulfilled if said processor comprises a processor specified by said locking condition.

19. A cache memory according to claim 17, wherein a processor has a type, and wherein said locking condition is fulfilled if a type of said processor comprises a processor type specified by said locking condition.

20. A cache memory according to claim 1, wherein said conditional access mechanism further comprises a cache invalidator, for invalidating data in specified cache memory sections.

21. A cache memory according to claim 1, wherein said cache memory comprises an associative memory.

22. A cache memory according to claim 21, wherein a cache memory section comprises a cache memory way.

23. A cache memory according to claim 1, wherein said cache memory comprises an n-way set associative memory.

24. A cache memory according to claim 23, wherein a cache memory section comprises an index of said n-way set associative cache memory.

25. A cache memory according to claim 1, wherein said cache memory comprises a direct-mapped memory.

26. A memory system comprising:

a main memory; and

a cache memory associated with said main memory, for caching data of said main memory, and having a conditional access mechanism configurable with a locking condition, for conditionally locking said cache memory.

27. A memory system according to claim 26, wherein said conditional access mechanism comprises:

a condition checker, for determining fulfillment of said locking condition;

a hit determiner, for giving hit and miss indications for data stored in said cache memory; and

a cache accessor, for conditionally implementing a cache memory access in accordance with the fulfillment of said locking condition.

28. A memory system according to claim 27, wherein said conditional access mechanism is operable to prevent replacement of data stored in a section of a conditionally locked cache memory.

29. A memory system according to claim 27, wherein said conditional access mechanism is operable to update data stored in a section of a conditionally locked cache memory.

30. A memory system according to claim 27, wherein said conditional access mechanism is operable to prevent reallocation of a section of a conditionally locked cache memory.

31. A memory system according to claim 27, wherein said conditional access mechanism is operable to access a section of a conditionally unlocked cache memory in accordance with a corresponding lock bit.

32. A memory system according to claim 26, wherein said locking condition is conditional upon at least one of the following group: a main memory address, a type of a memory access command, a processor, a processor type, and a locking indicator.

33. A memory system according to claim 26, associated with a processor operable to access said main memory via said cache memory.

34. A memory system according to claim 26, wherein said main memory comprises an embedded dynamic random access memory (EDRAM).

35. A processing system comprising:

a main memory;

a cache memory associated with said main memory, for caching data of said main memory, and having a conditional access mechanism configurable with a locking condition, for conditionally locking said cache memory; and

a processor associated with said cache memory, operable to access said main memory via said cache memory.

36. A processing system according to claim 35, wherein said conditional access mechanism comprises:

a condition checker, for determining fulfillment of said locking condition;

a hit determiner, for giving hit and miss indications for data stored in said cache memory; and

a cache accessor, for conditionally implementing a cache memory access in accordance with the fulfillment of said locking condition.

37. A processing system according to claim 36, wherein said conditional access mechanism is operable to prevent replacement of data stored in a section of a conditionally locked cache memory.

38. A processing system according to claim 36, wherein said conditional access mechanism is operable to update data stored in a section of a conditionally locked cache memory.

39. A processing system according to claim 36, wherein said conditional access mechanism is operable to prevent reallocation of a section of a conditionally locked cache memory.

40. A processing system according to claim 36, wherein said conditional access mechanism is operable to access a section of a conditionally unlocked cache memory in accordance with a corresponding lock bit.

41. A processing system according to claim 35, wherein said locking condition is conditional upon at least one of the following group: a main memory address, a type of a main memory access command, a processor, a processor type, and a locking indicator.

42. A method for conditionally locking a cache memory, said cache memory comprising multiple sections for caching the data of an associated main memory, comprising:

specifying a locking condition; and

performing conditional accesses to said cache memory in accordance with a main memory access command and the fulfillment of said locking condition.

43. A method for conditionally locking a cache memory according to claim 42, wherein said cache memory comprises lock bits corresponding to said sections, and wherein said performing comprises:

if said locking condition is fulfilled, accessing said cache memory with cached data locked; and

if said locking condition is not fulfilled, accessing said cache memory in accordance with said lock bits.

44. A method for conditionally locking a cache memory according to claim 42, wherein said locking condition is fulfilled if a currently accessed main memory location comprises a main memory location specified by said locking condition.

45. A method for conditionally locking a cache memory according to claim 42, wherein each main memory access instruction has a type, and wherein said locking condition is fulfilled if a type of said main memory access command comprises a command type specified by said locking condition.

46. A method for conditionally locking a cache memory according to claim 42, wherein said locking condition is fulfilled if a conditional locking indicator is set.

47. A method for conditionally locking a cache memory according to claim 42, wherein said main memory access command comprises a conditional locking parameter, and wherein said locking condition is fulfilled if said conditional locking parameter is set.

48. A method for conditionally locking a cache memory according to claim 42, wherein said main memory access commands originate from an associated processor.

49. A method for conditionally locking a cache memory according to claim 48, wherein said locking condition is fulfilled if said associated processor comprises a processor specified by said locking condition.

50. A method for conditionally locking a cache memory according to claim 48, wherein said locking condition is fulfilled if a type of said associated processor comprises a processor type specified by said locking condition.

51. A method for conditionally locking a cache memory according to claim 42, wherein said conditional accessing comprises preventing reallocation of a section of a conditionally locked cache memory.

52. A method for conditionally locking a cache memory according to claim 42, wherein said cache memory comprises lock bits corresponding to said sections, and wherein said conditional accessing comprises accessing a cache memory section in accordance with a corresponding lock bit, if said locking condition is not fulfilled.

53. A method for conditionally locking a cache memory according to claim 42, wherein said cache memory comprises lock bits corresponding to said sections, and wherein said conditional accessing comprises:

if a current cache access comprises a read access, performing a cache read operation to said cache memory;

if a current cache access comprises a write access, performing:

determining if said locking condition is fulfilled;

if said locking condition is fulfilled:

if a cache hit is obtained for a main memory location associated with said current cache access, performing a cache write operation to update cached data; and

if a cache miss is obtained for said location, performing a cache write operation with cached data locked against replacement; and

if said locking condition is not fulfilled, performing a cache write operation in accordance with said lock bits.

54. A method for conditionally locking a cache memory according to claim 42, further comprising specifying a parameter of said locking condition.

55. A method for conditionally locking a cache memory according to claim 42, further comprising updating said locking condition.

56. A method for conditionally locking a cache memory according to claim 42, further comprising invalidating data cached in said cache memory.